IN THE CLAIMS

Please amend the claims as shown below. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Currently Amended) A circuit for controlling the rise time of a signal, comprising:

a voltage multiplication circuit for converting an input voltage corresponding to said signal to an output voltage greater than said input voltage;

a ramp generator coupled to said voltage multiplication circuit for controlling said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator determines said rise time of said signal, wherein said signal comprises a staircase ramp signal; ~~and~~

a divide by N counter coupled to said ramp generator for generating a plurality of clock phases wherein said ramp generator is controlled with said clock phases; and

a keeper device coupled to said voltage multiplication circuit for allowing said voltage multiplication circuit to selectively hold said signal at said supply voltage and, upon enabling, to perform said converting.

2. (Original) The circuit of Claim 1, wherein said voltage multiplication circuit comprises a charge pump.

3. (Original) The circuit of Claim 1, wherein said signal is used to program and erase Flash EPROM cells.

4-6. (Cancelled)

7. (Previously Presented) The circuit of Claim 1 further comprising a level shifter.

8. (Original) The circuit of Claim 1 further comprising two non-overlapping clock signals.

9. (Previously Presented) The circuit of Claim 1 further comprising a ring oscillator coupled to said ramp generator.

10. (Previously Presented) The circuit of Claim 1 further comprising a capacitor divider network coupled to a switched capacitor network.

11. (Previously Presented) The circuit of Claim 10, wherein said switched capacitor network switches between ground potential and potential of a node of said capacitor divider network.

12. (Previously Presented) The circuit of Claim 11, wherein said node is coupled to a CMOS comparator.

13. (Cancelled)

14-16. (Cancelled)

17. (Currently Amended) A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump for converting an input voltage corresponding to said signal to an output voltage greater than said input voltage;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor network;

a regulator circuit coupled to said switched capacitor network ~~circuit~~ which causes a capacitor to switch between ground potential and the potential at a node, wherein a stair-step ramp signal is generated and said rise time is controlled with said switched capacitor, ~~wherein said switched capacitor controller performs a function related to programming a cell of said flash memory device, and~~ wherein said switched capacitor network comprises two capacitors wherein said rise time is controlled according to a ratio of capacitances of said two capacitors; ~~and~~

an oscillator coupled to said charge pump which generates an oscillating signal to said charge pump; and

a keeper device coupled to said charge pump for selectively allowing said charge pump to hold said signal at said supply voltage and, upon enabling, to perform said converting.

18. (Original) The switched capacitor controller of Claim 17 further comprising:

a divider coupled to said oscillator;

a non-overlapping two phase clock generator coupled to said divider.

19. (Previously Presented) The switched capacitor controller of Claim 17, wherein said ramp generator further comprises a capacitor divider network.

20. (Currently Amended) In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP for programming a cell of flash memory from a power supply via a ring oscillator, wherein said programming voltage is selectively greater than a supply voltage VCC from said power supply upon enabling and held to said supply voltage VCC without said enabling;

activating a program control signal PGM to enable programming of [[a]] said cell of said flash memory;

generating a stair-case ramp corresponding to ~~based on~~ said programming voltage VPP in response to said program control signal PGM, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

21. (Previously Presented) The method of Claim 20 further comprising switching a capacitor between ground potential and the potential at a node to generate said stair-case ramp.